Super Compact RFIC Inductors in 0.18μm CMOS with Copper Interconnects

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Abstract — **Design of super compact on-chip inductors with deep-shrunk dimension of 22μmx23μm, as opposed to several hundreds μm by several hundreds μm, is reported. Implemented in a 6-metal all-copper 0.18μm CMOS process, a flat inductor value of 10nH up to 4GHz, satisfactory to many typical RFIC applications, is achieved. The aggressive shrinkage reduces parasitic capacitance substantially and makes it realistic and cost-effective to realize sing-chip RFICs in very deep sub-micron technologies. A new inductor model is proposed for accuracy. A 2.4GHz LNA circuit with on-chip matching using the compact inductor is demonstrated.**

I. INTRODUCTION

There are growing interests in making high-quality on-chip inductors for low-cost radio frequency integral circuits (RFICs) [1]. Active research has been focusing on achieving high inductance value (L) and high quality factor (Q) IC inductors, typically using stacked spiral structures or MEMS techniques [2-6]. However, the large inductor size, typically a few hundreds micron by a few hundreds micron, and non-standard-process structures, result in large silicon consumption, intolerable capacitive effect and increased costs, making it unrealistic to design real single-chip RFIC chips, particularly for integration-intensive applications in very deep sub-micron regime. For single-chip RF applications, a super compact inductor with adequate inductance, flat over a large frequency spectrum, might be a better alternative to those non-CMOS, "perfect" inductors. This paper reports such a compact-size, stacked spiral inductor in standard CMOS featuring a flat L of 10nH with a 4GHz bandwidth in only 23x22μm^2. A Blutooth 2.4GHz LNA chip was designed using the super compact inductors.

II. COMPACT INDUCTOR

A. Spiral on-chip inductors

A typical single-layer on-chip spiral inductor is showed in Fig. 1. The equivalent inductance value could be obtained by several approaches [7], among them, a modified Wheeler formula follows:

$$L_{mw} = K_1 \mu \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{1}$$

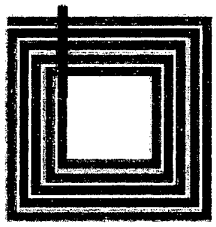

Fig. 1 Single-layer on-chip spiral inductor.

where K_1=2.34 and K_2=2.75 are layout dependent coefficients; d_{avg} is the average diameter of outer diameter and inner diameter; ρ is the fill ratio of the difference to the sum of the outer and inner diameters; n is spiral turns and μ is permittivity. From the definition of (2),

$$Q = \left. \frac{E_{stored}}{E_{diss}} \right|_{percycle} \tag{2}$$

the quality factor Q follows either,

$$Q = \frac{R_P}{\omega L} \cdot \left[1 - \left(\frac{\omega}{\omega_0} \right)^2 \right] = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} \tag{3}$$

or,

$$Q = \frac{\omega L}{R_s} \tag{4}$$

corresponding to a parallel or series RLC tank model. The Q decreases with serial resistance R_s. For a single spiral inductor, in order to obtain a relative inductance value, say 10nH, a large dimension (d_{avg}) is needed.

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B. Compact-size stacked spiral inductors

A vertical stacked-spiral inductor structure can achieve the same inductance value with a much smaller size. As shown in Fig. 2, a stacked structure can be easily constructed through using multiple interconnect layers in standard CMOS process. In this work, stacked-spiral inductors were fabricated using the UMC six-metal all-copper interconnect 0.18μm CMOS technology. The layout features of the inductor include six identical spirals, four turns per spiral, 1μm metal line width and 0.5μm line spacing, with a super compact planar dimension of only 22μm x 23μm.

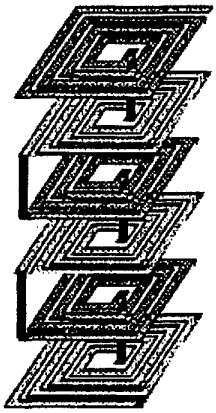

Fig. 2 A six-layer stacked spiral inductor.

In estimating the inductance value of a stacked-spiral inductor, the mutual coupling effect must be considered. Since the spiral dimension is generally several orders larger than dielectric thickness between any two metal layers, a good mutual coupling condition allows the inductance value of a two layer stacked structure be described by

$$L_{2-layers} = 2L + 2M = 2L(k+1) \tag{5}$$

where k is the coupling factor and very close to one, with identical spirals assumed. For multiple spiral structures, the L can be calculated by,

$$\frac{L_1}{L_2} = \frac{N_1^2}{N_2^2} \tag{6}$$

where N_1 and N_2 are layer counts of L_1 and L_2, respectively.

To reduce substrate-coupling effect, a grounded shield using a simple poly-silicon pattern between metal 1 and the substrate, is used as shown in Fig. 3 [8].

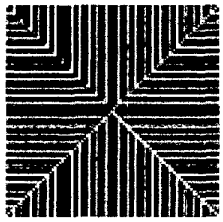

Fig. 3 A patterned poly-Si ground shield.

C. Modeling

To accurately calculate inductance of stacked-spiral inductors with mutual coupling effect considered, we propose a new inductor model, shown in Fig. 4 for a simple two-spiral inductor. An n-layer stacked-spiral inductor can then be modeled by adding top portion of the equivalent circuit, i.e., the L_N+L_{LN}, R_{SN}+R_{SCN}, $R_{via(N-1)N}$, and $C_{(N-1)N}$ network, layer by layer. The total equivalent series resistance and inductance are given by,

$$R_{eq} = \frac{R_S + R_{SC}}{\left(1-\omega^2(L+L_L)C\right)^2 + \left(\omega C(R_S + R_{SC})\right)^2} \tag{7}$$

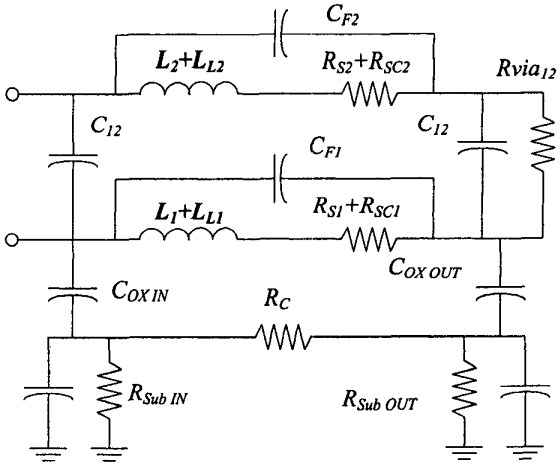

Fig. 4 A two-layer stacked inductor equivalent circuit.

and

$$L_{eq} = \frac{1}{2\pi f} \cdot \frac{\omega(L+L_L)\left(1-\omega^2(L+L_L)C - \dfrac{C(R_S+R_{SC})^2}{L+L_L}\right)}{\left(1-\omega^2(L+L_L)C\right)^2 + \left(\omega C(R_S+R_{SC})\right)^2} \tag{8}$$

The equivalent substrate coupling admittance Y_{SUBIN} is given by,

$$Y_{SUB_{IN}} = \frac{R_{SUB_{IN}} C_{OX_{IN}} \omega\left(C_{OX_{IN}} + C_{SUB_{IN}}(1-\omega)\right)}{1 + R_{SUB_{IN}}^2 \omega^2 \left(C_{OX_{IN}} + C_{SUB_{IN}}\right)^2}$$

$$+ j\frac{C_{OX_{IN}} \omega\left(1 + R_{SUB_{IN}}^2 C_{SUB_{IN}}\left(C_{OX_{IN}} + C_{SUB_{IN}}\right)\omega\right)}{1 + R_{SUB_{IN}}^2 \omega^2 \left(C_{OX_{IN}} + C_{SUB_{IN}}\right)^2} \tag{9}$$

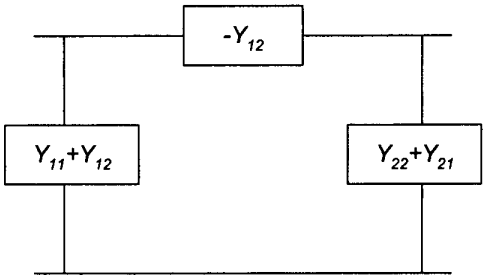

Fig. 5 A y-parameter π-model for L-measurement.

D. Measurements

The y-parameters are measured using equivalent π-model as depicted in Fig. 5. By taking the real and imaginary parts of y_{12}, equivalent inductance and resistance can be extracted as,

$$y_{11} = \frac{1 - s_{11} + s_{22} - |s|}{1 + s_{11} + s_{22} + |s|} \qquad y_{12} = \frac{-2s_{12}}{1 + s_{11} + s_{22} + |s|}$$

$$R = \frac{-50 \cdot \mathrm{Re}(y_{12})}{\mathrm{Re}(y_{12})^2 + \mathrm{Im}(y_{12})^2} \tag{10}$$

$$L_1 = \frac{1}{2\pi f} \cdot \frac{50 \cdot \mathrm{Im}(y_{12})}{\mathrm{Re}(y_{12})^2 + \mathrm{Im}(y_{12})^2} \tag{11}$$

$$Q = \frac{-\mathrm{Im}(y_{11})}{\mathrm{Re}(y_{11})} \tag{12}$$

Although equation (11) is widely used, its inductance is not extracted physically and contains the capacitive coupling, resulting in over-evaluation of inductance at higher frequency. Alternatively, L can be extracted from y_{11} data using the following equation to avoid the high frequency over shoot

$$L_2 = \frac{1}{2\pi f} \cdot \frac{-50 \cdot \mathrm{Im}(y_{11})}{\mathrm{Re}(y_{11})^2 + \mathrm{Im}(y_{11})^2} \tag{13}$$

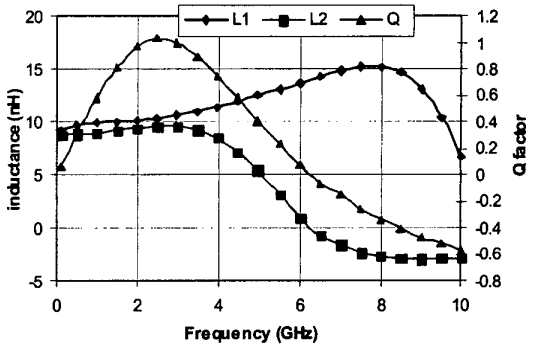

Fig. 6. Test data of a 6-layer compact-size stacked-spiral inductor with identical spirals, 4 turns per spiral, 1μm metal width and 0.5μm spacing.

The extracted inductance data using both approaches (i.e., L1 and L2) are shown in Fig. 6 along with Q-factor. It is observed that the two extracted inductance values matches each other well at low frequency region, while over-shoot in L1 is evident at high frequency. As designed, good inductance values of about 10nH (L_{1avg}=*10nH and* L_{2avg}=*9.33nH*) are achieved, which are fairly flat over a wide frequency spectrum up to 4GHz. These inductor specifications are generally adequate for many single-chip RFIC chips. Compare with simulation value of L_{sim}=9.75nH, the error margin is less than 5% in this design. A peak Q factor of 1.10 at 2.48GHz is obtained, which is apparently low compared to many reported data with focus on achieving high Q using MEMS techniques. The root cause for low-Q in this design comes from high resistive losses due to narrow metal line width of 1μm, designed to realize the super compact 22μm x 23μm size. Relative thinner metal thickness of the process used is another factor. Low Q factor apparently has adverse impact. However, considering the compact size and adequate inductance value using copper interconnects, therefore a very high L-to-size ratio achieved, the new compact inductor could be a good solution to single-chip design that satisfies most critical RF circuit specifications as demonstrated by the 2.4GHz LNA circuit discussed next. Currently, we are working to improve the Q-factor using a novel close-loop magnetic technique.

II. AN 2.4GHZ LNA DESIGNED USING COMPACT SIZED INDUCTOR

LNA circuit is one of the most fundamental modules of RFICs. However, real monolithic LNA is difficult to design because of the large size inductors needed, typically with a dimension of several hundreds micrometers each side for a reasonable inductance. An area-efficient single-chip 2.4 GHz bluetooth LAN chip was designed with complete on-chip impedance matching using the compact inductors. Fig. 7 shows the LNA schematic consists of four transistors and four inductors. The required inductors are L_1=13nH, L_2=1.2nH, L_3=1.2nH, and L_4=20nH. Typically, it was unrealistic to put a large inductor of 15-20nH on chip if a traditional fat spiral inductor is used because it consumes too much Si and produces too much capacitive effect. However, using the new super compact inductors, a realistic monolithic LNA circuit with satisfied circuit specifications can be realized. The extracted S_{21} vs. frequency curve for the LNA is given in Fig. 8. Critical LNA parameters obtained are the gain of 23.35dB, central frequency of 2.4GHz and the bandwidth is 900MHz. All of them meet the design requirements.

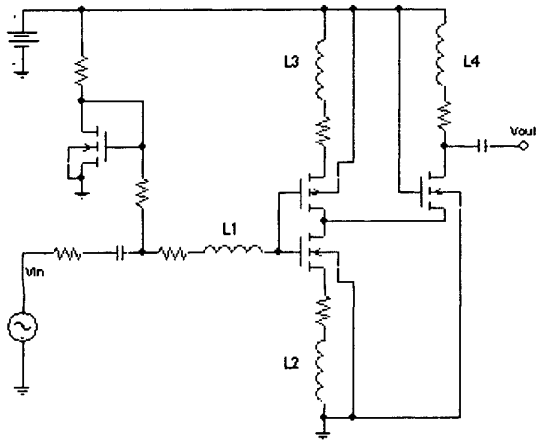

Fig. 7 A schematic of a 2.4GHz LNA circuit.

III. CONCLUSION

A super compact, stacked-spiral inductor is designed and fabricated in a commercial 6-metal all-Cu interconnect 0.18μm CMOS technology. The design achieves a high and very flat inductance of 10nH with a 4GHz bandwidth in a 22μm x 23μm size. These values meet the needs of many RFIC chips as demonstrated by a 2.4GHz LNA circuit. A new inductor model is proposed for accurate inductance evaluation. The relative Q-factor can be improved by reducing magnetic losses. This compact inductor is proven to be a satisfactory solution for realistic single-ship RFICs, particularly for integration-incentive applications in very deep sub-micro regime

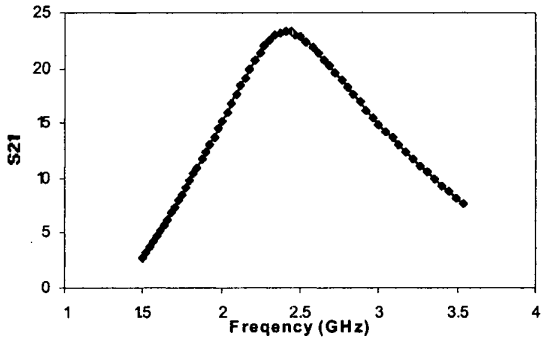

Fig. 8 Extracted S21 curve for the 2.4GHz LNA circuit.

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